SCOPE OF ACCREDITATION

Electronics

Eltek Ltd
Galis 20 Street
Petach-Tikva, 49101
Israel

This certificate expiration is updated based on periodic audits. The current expiration date and scope of accreditation are listed at: www.eAuditNet.com - Online QML (Qualified Manufacturer Listing).

In recognition of the successful completion of the PRI evaluation process, accreditation is granted to this facility to perform the following:

AC7119 Rev G - Nadcap Audit Criteria for Electronics Printed Boards (to be used on audits on/after 5 March 2017)

10– Oxide Coating / Oxide Replacement Coating
11– Material Lay–Up and Lamination
12.1– Drilling: Mechanical Drilling
12.2– Drilling: Laser Drilling– In House
12.4– Drilling: Post–Drill Cleaning and Etchback
13.1– Cooper Plating: Electroless Copper/Direct Metallization
13.2– Copper Plating: Electroplated Copper
14.1– Final Finishes: Hot Air Solder Leveling (HASL)
14.3a– Final Finishes: Electroless (Chemical)/Immersion Plating Final Finish – ENIG
14.3c– Final Finishes: Electroless (Chemical)/Immersion Plating Final Finish – Immersion Silver
14.3– Final Finishes: Electroless (Chemical)/Immersion Plating Final Finish
14.4a– Electroplated Final Finishes: Electroplated Nickel–Gold
14.4b– Final Finishes: Electroplated Gold
14.4d– Final Finishes: Electroplated Nickel
14.6– Final Finishes: Wire Bondable Plating
15– Legend and Marking
16– Routing and Machining
17– Electrical Test – Functional
18– X–Ray Fluorescence (XRF)
19– Microsection Sample Selection, Preparation, and Inspection
20– Structural Integrity
21– Materials Lab

22– Chemistry Lab
23– Monthly Quality Conformance Testing
24– Final Validation
25– Packaging
6– Engineering Source File Processing
7.1– Material Control: General
7.2– Material Control: PrePreg
8.1– Imaging – Photoprocess
8.2.1– DES – Developing Photoimageable Resist
8.2.2– DES – Copper Etching of Inner Layers and Outer Layers
8.2.3– DES – Stripping of Resist Film and Etch–Resist Plating
8.2– Imaging – Develop–Etch–Strip (DES) and Strip–Etch–Strip (SES)
8.3– Etched Image Inspection (Manual or AOI)
9.1– Permanent Solder Mask: Solder Mask Application
9.2– Permanent Solder Mask: Solder Mask Exposing
9.3– Permanent Solder Mask: Solder Mask Develop and Cure
9– Permanent Solder Mask

AC7119/2 Rev A - Nadcap Audit Criteria for Electronics Flexible and Rigid-Flexible Printed Boards (to be used on audits on/after 5 March 2017)

04– Handling
05– Material
06– Cover Material Application
07– Post–Drill Cleaning and Etchback
08– Stiffener Bonding
09– Strain Relief
10– Testing
11– Depanelization
12– Packaging
13– Final Validation

AC7119/3 - Nadcap Audit Criteria for Electronics High Density Interconnect Printed Boards

05.1– Hole Filling Material Control: Conductive Hole Fill Material for Blind and Buried Vias
05.2– Hole Filling Material Control: Non Conductive Hole Fill Material for Blind and Buried Vias
06– Inner Layers Registration
07– Material Lamination
08.1– Drilling: Mechanical Drilling
08.2– Drilling: Laser Drilling
09.1–Via Hole Filling Process
09.2– Via Hole Filling Process: Oxide Coating / Oxide Replacement Coating
09.3– Via Hole Filling Process: Buried Via Hole Filling Process

09.4– Via Hole Filling Process: Blind Via Hole Filling Process
10.1– Final Validation: General
10.2– Final Validation: Lifted Lands
10.3– Final Validation: Workmanship (shop floor)
10.4.1– Final Validation: Dimensional Requirements: Hole Pattern Accuracy
10.4.2– Final Validation: Dimensional Requirements: Registration (Internal)
10.4.3– Final Validation: Dimensional Requirements: Annular Ring (External)
10.5.1– Final Validation: Conductor Definition: Conductor Width
10.6.1– Final Validation: Structural Integrity: Microvia Integrity
10.6.2– Final Validation: Structural Integrity: Filled Vias