

# Material Selection & Technology Processes for 5G Systems

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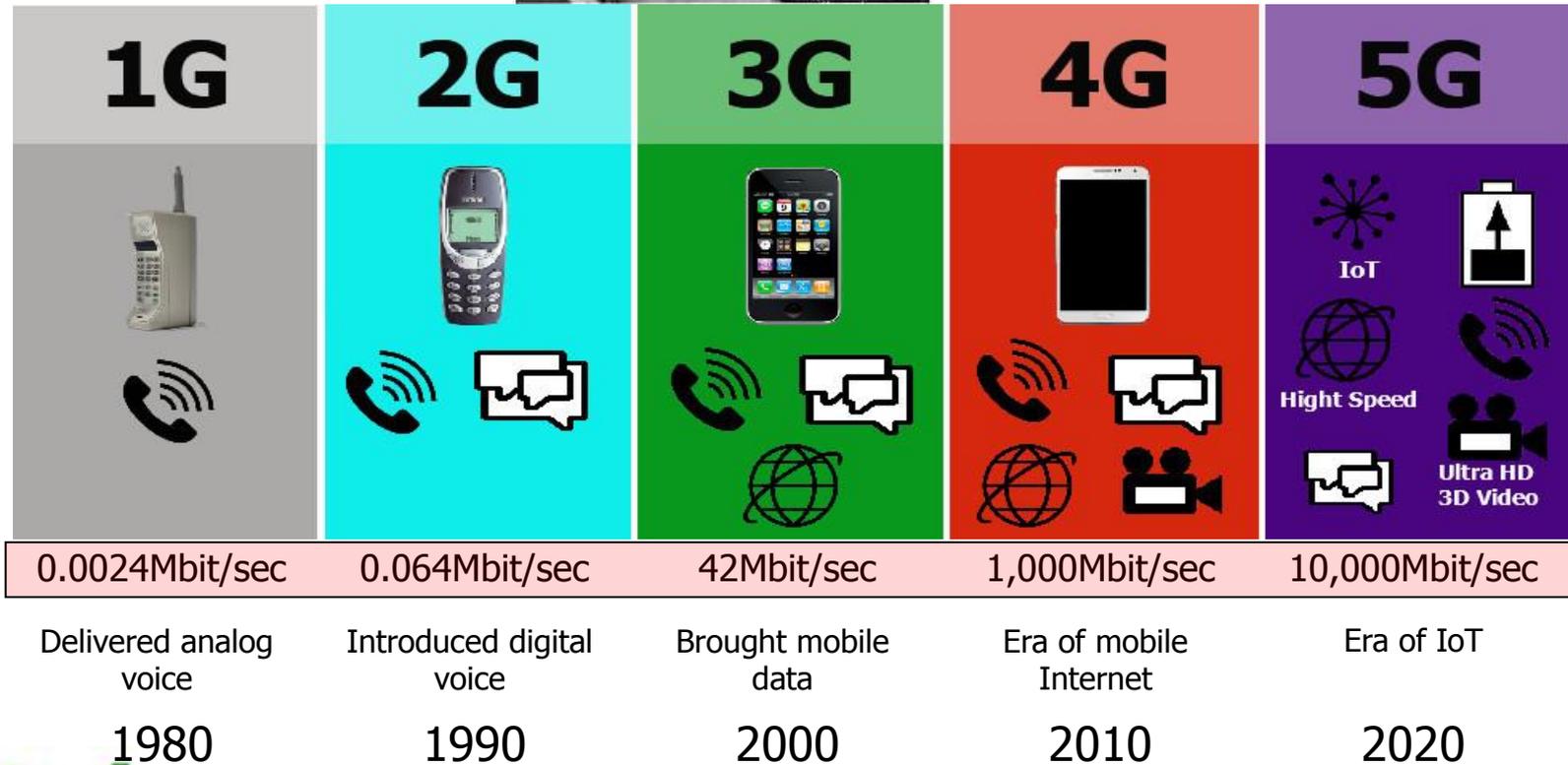


# The Mobile Wireless Communication Technology



**0G**

1946



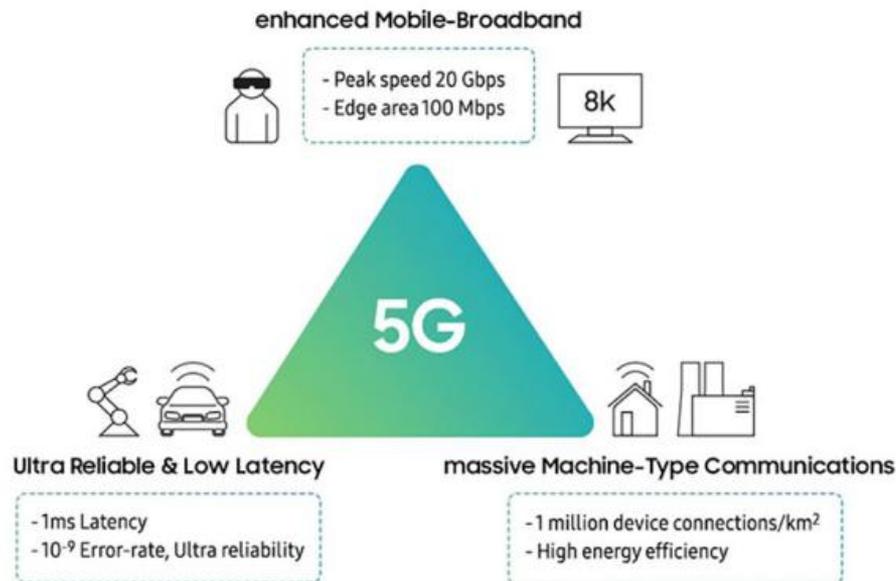
# What is 5G ?

**5G is the 5th generation mobile network. It will take a much larger role than previous generations.**

5G will elevate the mobile network to not only interconnect people, but also **interconnect and control machines, objects, and devices.**

## 5G benefits:

- ✓ deliver multi-Gbps peak rates
- ✓ ultra-low latency
- ✓ massive capacity



[7]

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# 5G and PCB Materials

Overall, 5G is a complex system and PCB is necessary in every constituent hardware part.

**The main development directions of PCB in the 5G era are multilayer applications, high frequency, high speed, high density, rigid-flex and mixed high and low frequencies.**

Traditional epoxy resin copper clad laminate (CCL) cannot meet the high frequency requirement of 5G environments.

In the 5G era millimeter-wave band between 30 GHz and 300 GHz will be put into use to improve the wireless data capacity.[4]

**The PTFE CCL is an excellent dielectric material with a low dielectric constant and minimal dielectric loss and has many applications.** It can be widely used in mobile communication equipment, radio receivers, transfer devices, base station antennae, and consumers electronics.

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## Selection PCB Materials for 5G

Choosing a circuit material for a high-frequency PCB is generally a tradeoff, often between price and performance.

But PCB materials are also selected by two key factors:

- ✓ how well they meet the needs of an end-use application
- ✓ what kind of effort is required to fabricate a desired circuit with a particular material. [3]

Material	Ease of Circuit Fabrication	Electrical Performance
PTFE with micro glass fiber	Difficult	Excellent
PTFE with woven glass	Difficult	Good
Ceramic - filled PTFE	Moderate	Excellent
Ceramic-filled PTFE with woven glass	Moderate	Good
Ceramic-filled Hydrocarbon	Difficult	Good
Ceramic-filled Hydrocarbon with woven glass	Easy	Good
High Performance FR-4	Easy	Poor

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# Choosing Materials Based on Circuit Fabrication Issues

A number of different mechanical processes are required as part of high-frequency PCB fabrication. In general, the most critical of these would be:

- ✓ Multilayer Lamination
- ✓ Drilling
- ✓ Plated-Through-Hole (PTH) Preparation
- ✓ Assembly

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# Choosing Materials Based on Circuit Fabrication Issues

## Drilling and PTH Preparation

The drilling process is typically concerned with creating clean holes, which will later be metalized to form VIA-holes for electrical connections from one conductive layer to another.

Some concerns with the drilling process include:

- ✓ Smear - smearing can be lethal to PCB fabrication using a PTFE based material, since there is no way to remove the smear.
- ✓ Burring- can lead to reduce hole diameter and could be a trigger to mechanical and electrical fails in thermal cycles.
- ✓ Fracturing of the material - fracturing can be fatal for some of the nonwoven glass and hydrocarbon materials.

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# Choosing Materials Based on Circuit Fabrication Issues

## Multilayer Lamination and Assembly

Fabricating multilayer PCBs presents many challenges.

One is the fact that dissimilar materials are often being bonded together, and these dissimilar materials can have properties which complicate drilling and PTH preparation processes.

Also, a mismatch between certain material properties, such as coefficient of thermal expansion (CTE), can lead to reliability problems when the circuit is thermally stressed during assembly.

A goal of the material selection process is to find a good combination of circuit materials for a multilayer PCB which enable practical fabrication processing while also meeting end-use requirements. [3]

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# Choosing Materials Based on Circuit Fabrication Issues

Designers and fabricators have many choices of materials used to bond together the copper-clad laminates that ultimately form a multilayer PCB. [3]

Bonding Materials	Dk	Df	Lamination Temperature [°C]	Preparation for PTH	Re-melting Temperature [°C]
Glass Microfiber Reinforced PTFE	2.2	0.0009	390	Special	337
FEP (Fluorinated ethylene propylene)	2.1	0.0010	296	Special	271
Ceramic-filled PTFE, Dk=3	3.00	0.0013	371	Special	337
Ceramic-filled PTFE, Dk=6	6.15	0.0020	371	Special	337
Ceramic-filled PTFE, Dk=10	10.80	0.0023	371	Special	337
LCP	2.90	0.0025	290	Special	271
3001	2.30	0.0030	218	Special	176
Thermoset Hydrocarbo	3.90	0.0040	176	Standard	N/A
FR-4	4.50	0.0180	182	Standard	N/A



# Choosing Materials Based on Circuit Fabrication Issues

The greatest concern during PCB assembly is due to the effects of thermal stress from soldering.

In terms of circuit materials, effects from thermal stress can typically be projected by comparing the CTE values for different materials. [3]

Material	CTE (ppm/°C)	Electrical Performance
PTFE with micro glass fiber	220	Excellent
PTFE with woven glass	200	Good
Ceramic-filled PTFE	25	Excellent
Ceramic-filled PTFE with woven glass	50	Good
Ceramic-filled Hydrocarbon	20	Good
Ceramic-filled Hydrocarbon with woven glass	35	Good
High Performance FR-4	50	Poor

In general, a circuit material with a lower CTE will be more robust and handle the thermal stress better than a material with a higher overall CTE.

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# Choosing Materials Based on Circuit Fabrication Issues

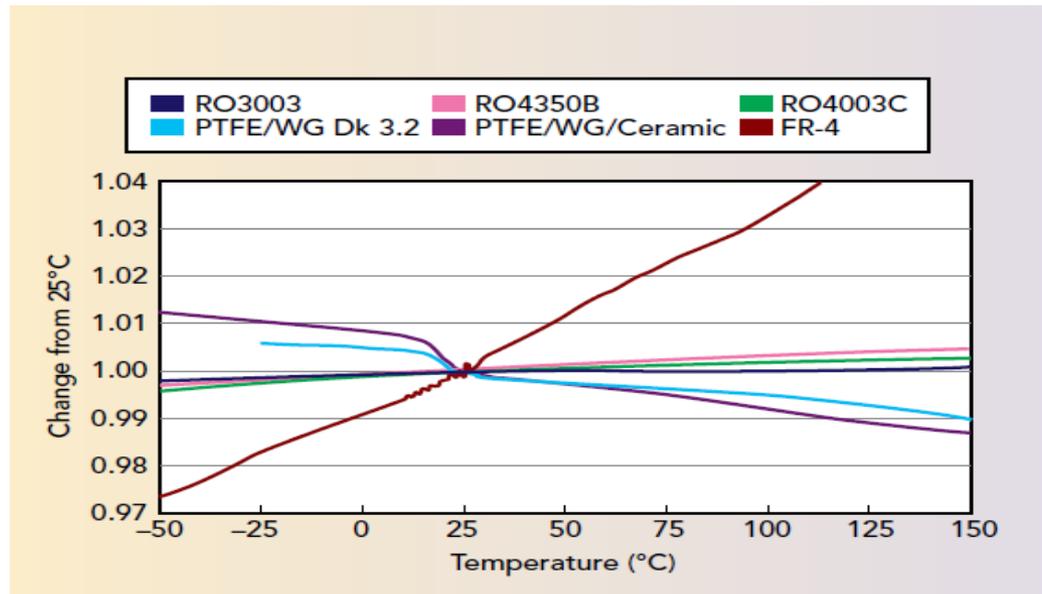
## Thermal Conductivity

The heat generated by the 5G PCB is often related to insertion loss. Basically, a circuit with higher insertion loss will generate more heat. Using a high-frequency materials that has a high thermal conductivity can be very beneficial to the thermal management 5G application. [8]

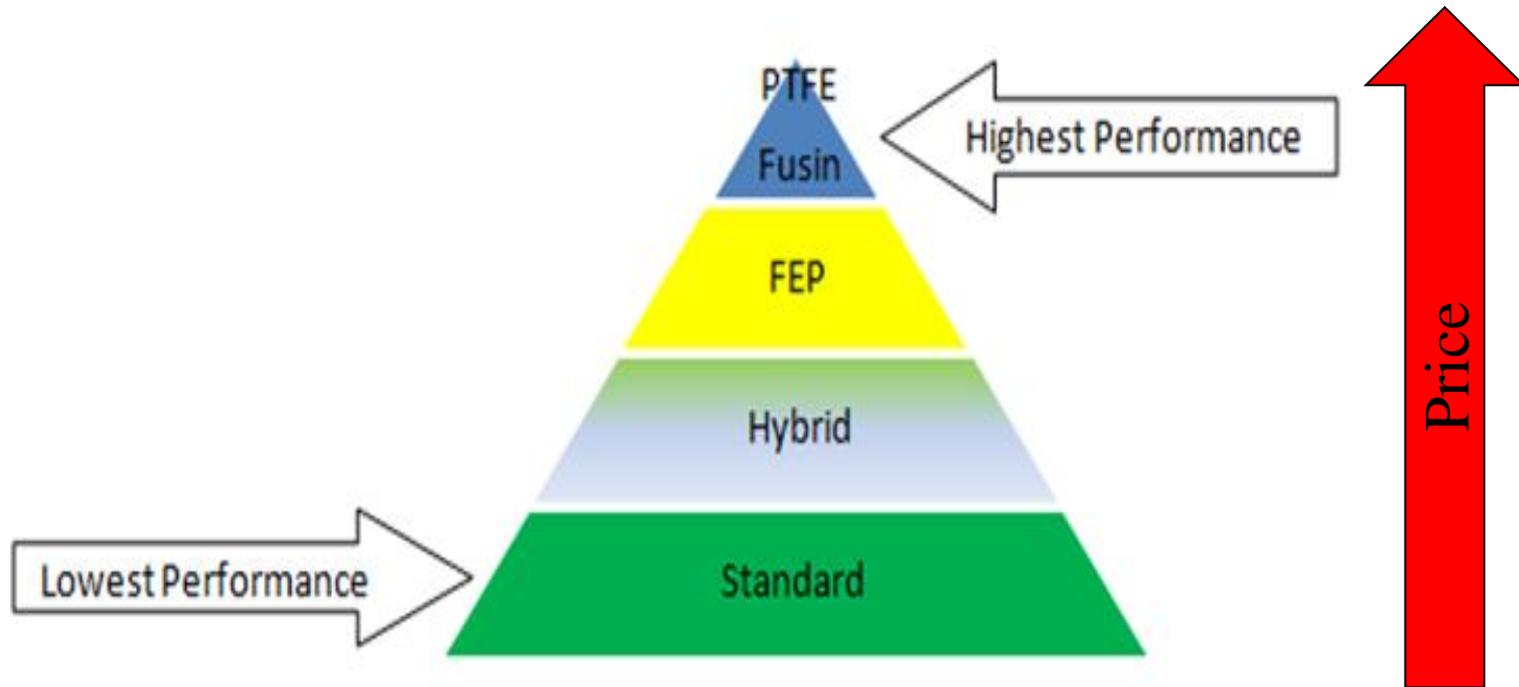
Product	Dk, @ 10 GHz	Df @ 10 GHz	Thermal Coefficient of Dk -50°C to 150°C ppm/°C	Coefficient of Thermal Expansion -55° to 288°C ppm/°C (X/Y/Z)	Thermal Conductivity W/(m•K) (50°C)	Water Absorption 50 %
<b>CLTE™</b> Woven Glass Reinforced PTFE	2.98±0.04	0.0023	-9	10/12/34	0.50	0.04
<b>RO1200™</b> PTFE Ceramic Woven Glass Reinforced	3.05±0.10	0.0017	NA	8/8/30	0.42	0.03
<b>RO3003™</b> PTFE Ceramic	3.00±0.04	0.0010	-3	17/16/25	0.50	0.04
<b>RT/duroid 5880</b> PTFE Random Glass Fiber	2.20±0.02	0.0009	-125	31/48/237	0.20	0.02
<b>RO4350B™</b> Hydrocarbon Ceramic Woven Glass	3.48±0.05	0.0037	+50	10/12/32	0.69	0.05

# Environment Changes Affect on Dk and Df

	Competitor I			RO3003™ laminate		
LSL Testing	Dk @ 10 GHz	Df @ 10 GHz	Moisture absorb (%)	Dk @ 10 GHz	Df @ 10 GHz	Moisture absorb (%)
23°C, 50% RH	2.97	0.0036	baseline	2.97	0.0014	baseline
24 hrs in 23°C water	3.00	0.0057	0.24	2.98	0.0021	0.05
72 hrs at 85°C, 85% RH	3.00	0.0046	0.19	2.98	0.0018	0.02



# High Electrical Performance Compare to Other Lamination Methods



[6]

The fabricating PTFE-based multilayer circuits can require special handling of the circuit materials for optimum results. [1]

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# Fusion Bonding Using PTFE Composite Materials

## Fusion bonding PTFE materials

Requires to uses high temperature ( $>325^{\circ}\text{C}$ , typically  $370^{\circ}\text{C}$ ) and often high pressure (250-1700 PSI) for melting & re-crystallization of PTFE materials while held under pressure.

## Benefits of process:

- ✓ Homogenous multi-layer constructions using high performance materials (low Dk, low Df, uniform CTE).
- ✓ Improved layer-layer registration as compared to MLB's bonded using low temperature thermosetting modified PTFE prepreg and Non-PTFE materials .
- ✓ Excellent dielectric layer to layer adhesion.
- ✓ Highly reliable MLB structure.

## Disadvantage of process:

- ✓ No sequential lamination.
- ✓ No cavity design.
- ✓ No foil lamination.

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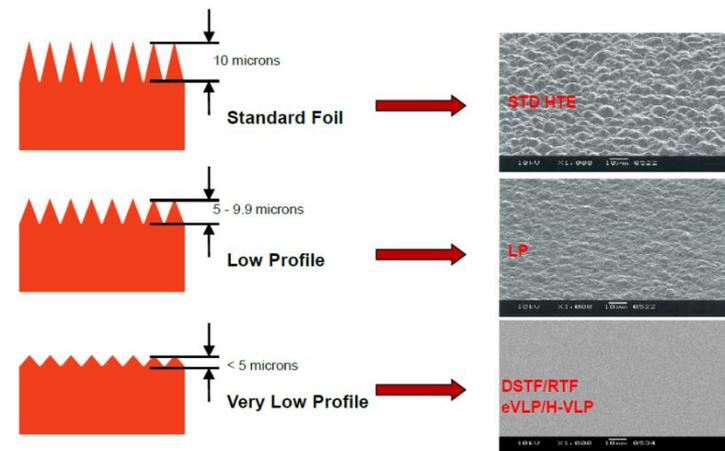
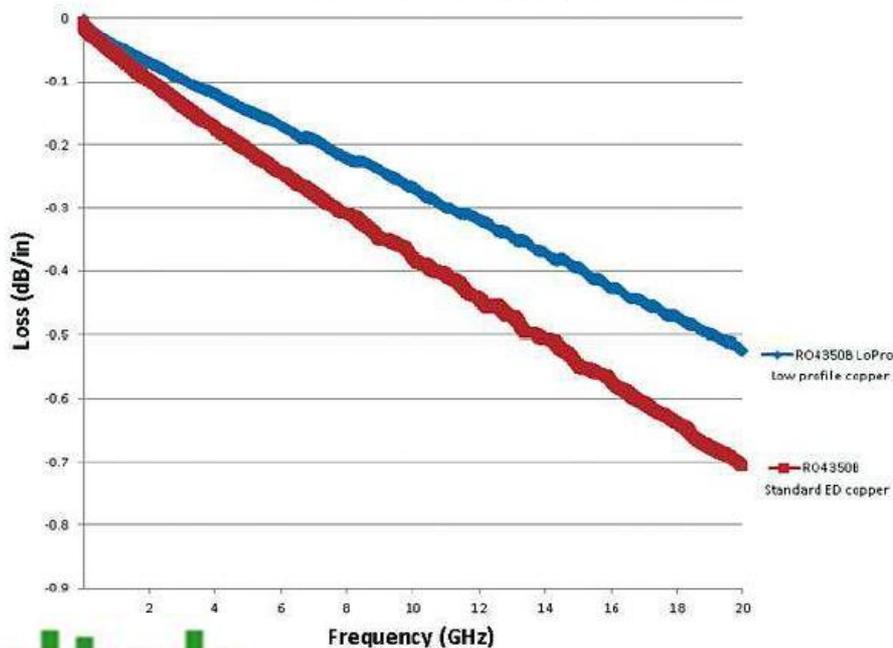
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# Conductor Losses

In addition to dielectric losses, conductor losses are important when comparing circuit materials. Especially for thin circuits, conductor losses can be more significant than dielectric losses.

Conductor losses can be impacted by circuit design, circuit configuration, and the thickness of conductive metals, as well as the surface roughness of the copper conductor layers. [3]

Insertion Loss, 10mil thick, 50 ohm Microstrip, Copper type comparisons



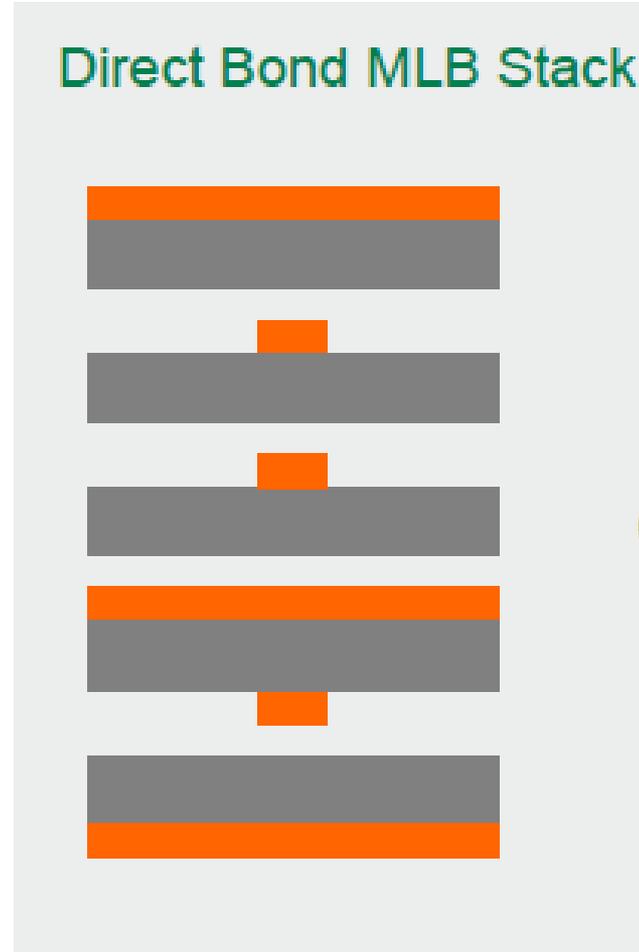
Source: Isola

# Fusion Bonding Using PTFE Composite Materials

## Direct Bonding:

- ✓ Bonding together pressed (densified) cores (require to use high pressure as 1000-1700 PSI)
- ✓ Requires use of fully etched surfaces against copper-pattern inner-layer (prohibited vertical stacking of copper on opposing layers)
- ✓ May require fully etched “spacer” core between opposing copper layers

## Direct Bond MLB Stack



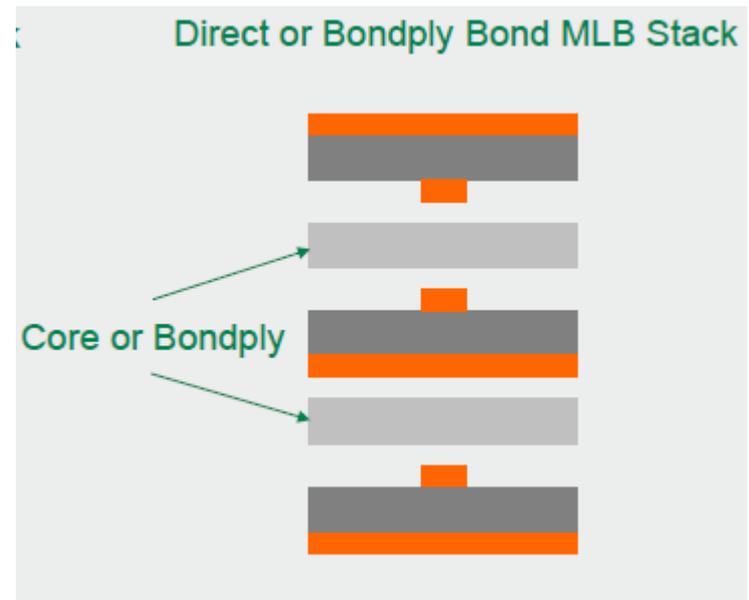
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# Fusion Bonding Using PTFE Composite Materials

## Bondply Bonding:

- ✓ Uses undensified (“unpressed”) layers of RT/duroid 6002™ or RO3000® materials between opposing core layers
- ✓ Traditional core/adhesive/core MLB stack-up (Bondply layers used similar to core layers during fusion bond process. Bondply ply bonding make better fill and therefore require lower pressure such 400-500 PSI)



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# Direct vs. BondPly PTFE Fusion Bonding

## Benefits of BondPly Bonding

- ✓ Encapsulation of buried features
- ✓ Resolved conductor compression into core layers
- ✓ Less lamination temperature and pressure

## Disadvantages of BondPly Bonding

- ✓ Less uniformity (Dk, Df, CTE)

## Benefits of Direct Bonding

- ✓ Uniformity of Z-axis spacing
- ✓ High uniformity (Dk, Df, CTE)

## Disadvantages of Direct Bonding

- ✓ High lamination temperature and pressure

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# Eltek BondPly StackUp RT6002+RO3003

 a Nistec company	ELTEK NO.	EL-F4639		
	CUSTOMER P/N:		REV	
	PCB	PCB+HS		
Required Thick (inch)	0.0470			
Required Tolerance(+)	10%			
Required Tolerance(-)	10%			
Measured epoxy/con	0			(conductor = 0, epoxy=1)
	Final	HS+	After Pre.	
אין לגעת	Max.	0.0517	0.0000	0.0457
		0.0423	0.0000	0.0393
בשורה	Nominal Before Plating			0.0425
חסמה	Design			0.0432
		HS	PP	PCB+HS design
		0.0000	0.0000	0.0000
				..OLD MASTER\Eltek-Material.XLS

DATE	05.05.19
UP DATE	

	Layer	.Cu (OZ)	CORE Thickness (inch)	Quantity	Prep	Dielec Req	remark	drill kind	Control & Note's
	No				Descr				
	1	CS	0.5						
1/2	CORE		0.01				RT6002		
	2	G	0.5						
	PP			1	0.005		RO3003		
	3	S	0.5						
3/PD3	CORE		0.01				RT6002		
	PD3	0	0						
	PP			1	0.005		RO3003		
	4	G	0.5						
4/5	CORE		0.01				RT6002		
	5	PS	0.5						

RT6002 @ 10GHz Dk 2.94±0.04; Df 0.0012

RO3003 @ 10GHz Dk 3.00±0.04; Df 0.0010

Press temperature 370°C

Pressure 500 PSI

# Eltek BondPly StackUp RT6002+RO3003

## CROSS SECTION REPORT

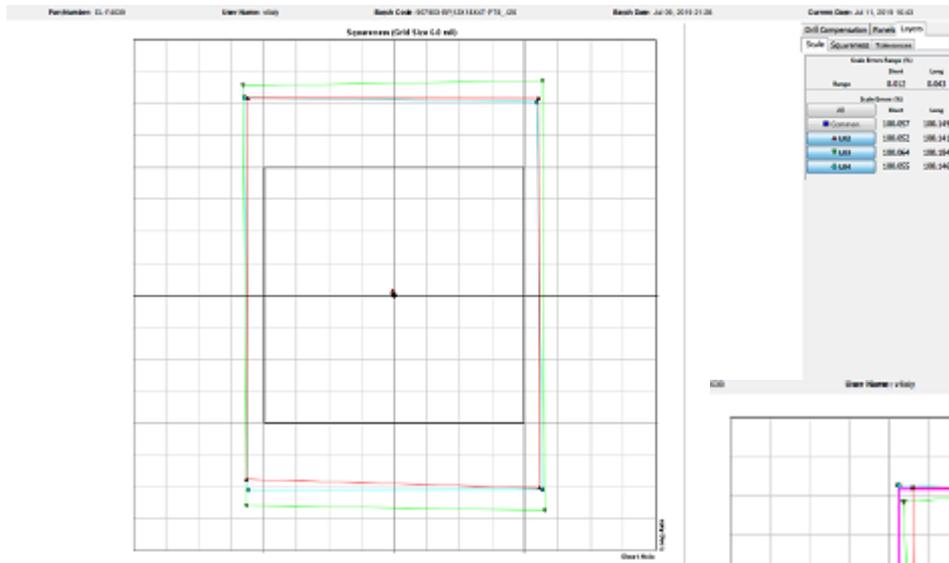
Customer Name: EL-F4635 Part No.: 907903 Rev: \_\_\_\_\_  
 Eltek No.: \_\_\_\_\_ Date Code: \_\_\_\_\_ Sample No.: \_\_\_\_\_  
 Total Thickness – Designed: 0.0432" Measured: 0.0419"

### Construction

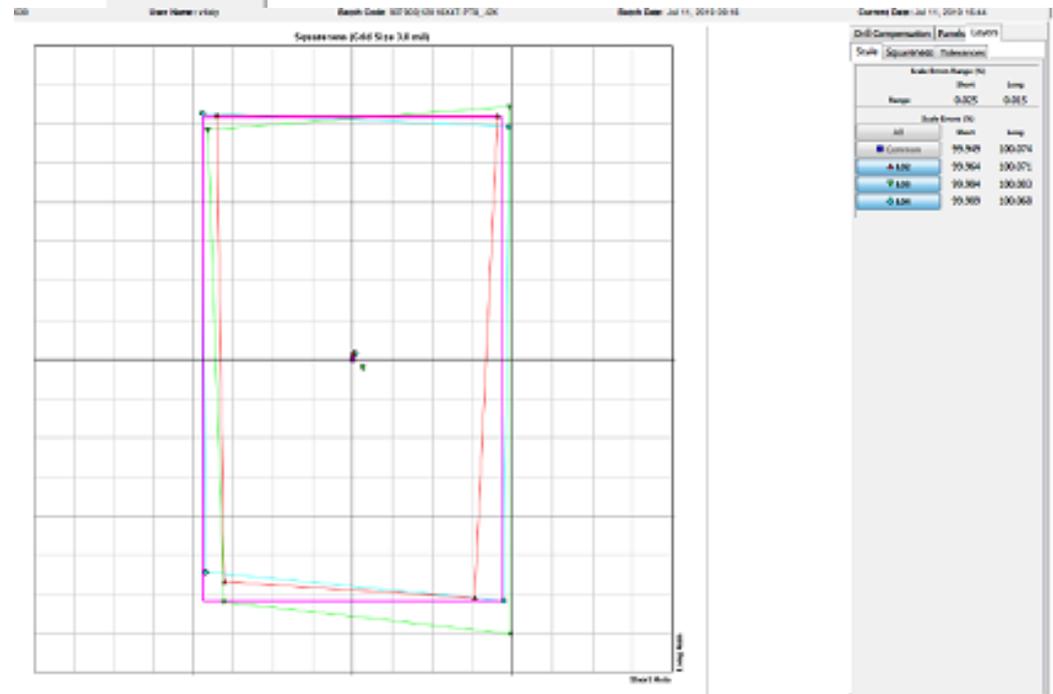
	Layer	Layer	.Cu (OZ)	CORE Thickness (inch)	Quantity	Prep
	No	Descr				Thick
						(inch)
	1	CS	0.5			
1/2	CORE		0.01			
	2	G	0.5			
	PP			1	0.005	
	3	S	0.5			
3/PD3	CORE		0.01			
	PD3	0	0			
	PP			1	0.005	
	4	G	0.5			
4/5	CORE		0.01			
	5	PS	0.5			

	Designed (µm)		Measured (µm)	
	Copper Layer	Dielectric	Copper Layer	Dielectric
1				
2		254		250
3		127		115
4		381		366
5		254		244
6				
7				
8				

# Registration RT6002+RO3003

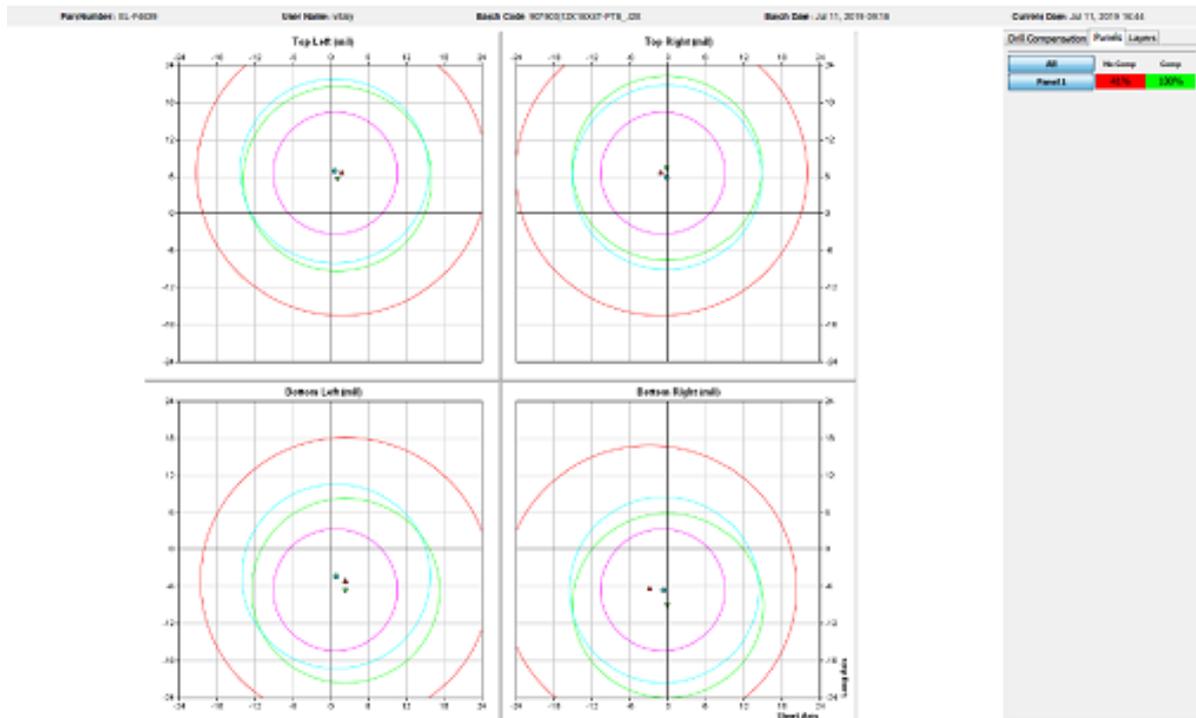


Before Lamination



After Press

# Registration RT6002+RO3003



After Press

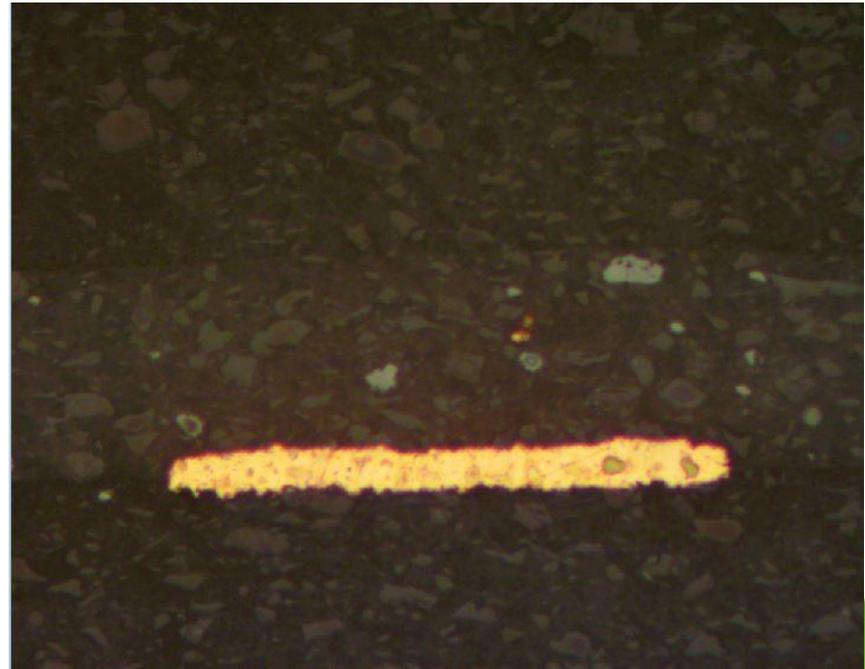
...

- ✓ Good centering position
- ✓ Good layer to layer registration

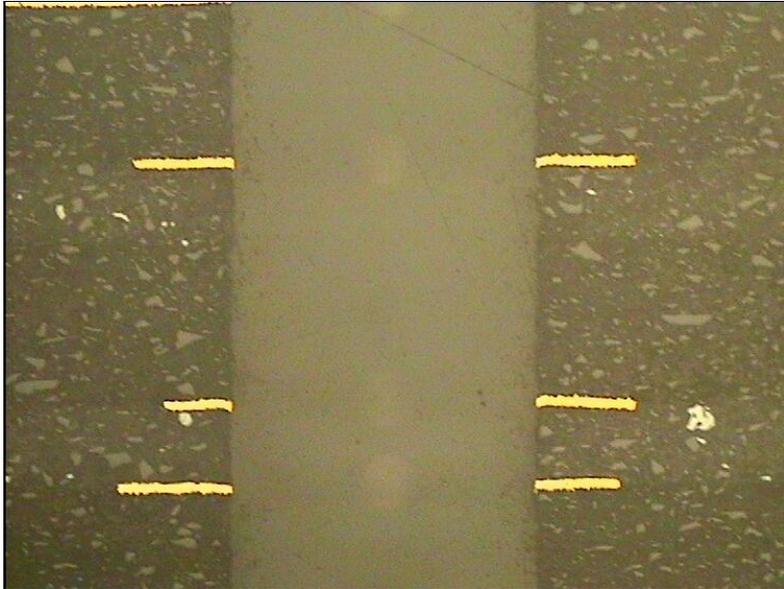
# Coupon Tests RT6002+RO3003



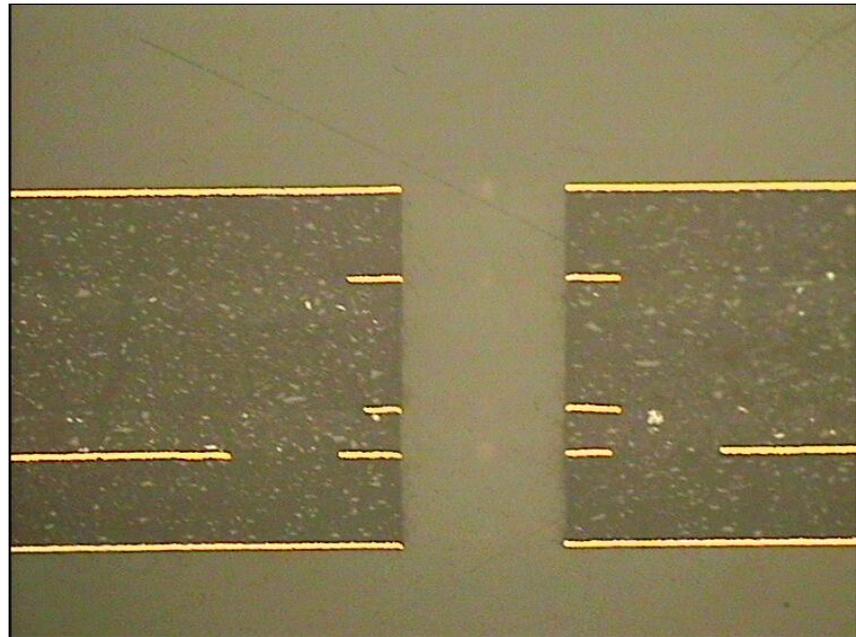
After Press



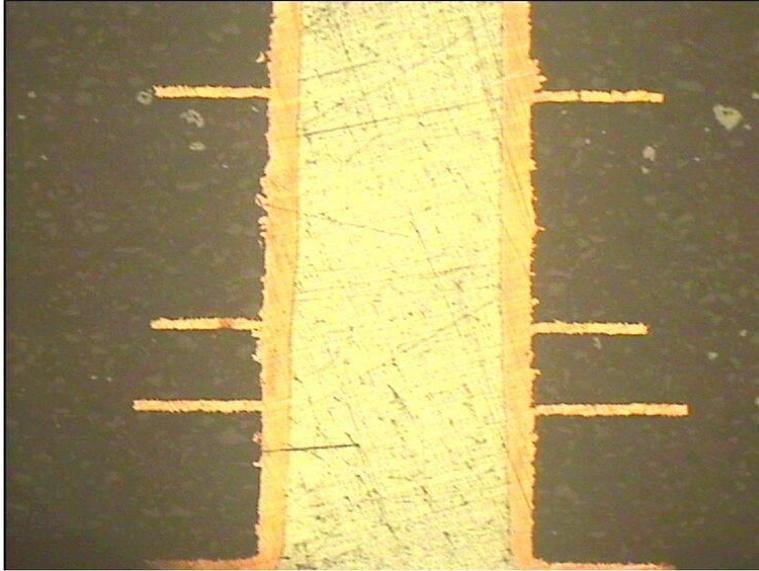
# Coupon Tests RT6002+RO3003



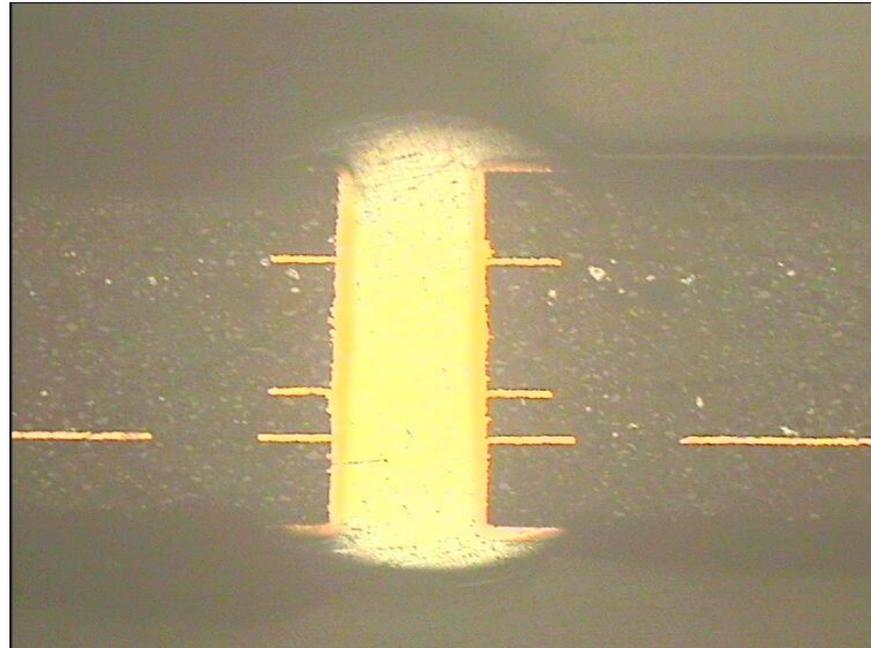
After Drill



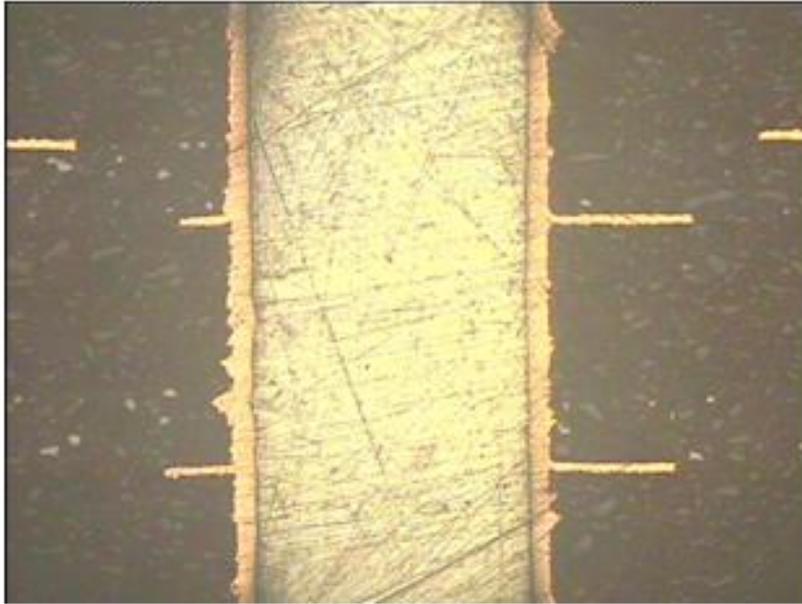
# Coupon Tests RT6002+RO3003



After 3 Thermal Stresses  
@285°C x 10 sec x 3 times



# Coupon Tests RT6002+RO3003



After 6 Thermal Stresses  
@285°C x 10 sec x 6 times



# Eltek Direct Bonding StackUp RT5880

 a  company	ELTEK NO.	EL-F5703		
	CUSTOMER P/N:	PTFE Fusion Bonding	REV	-
	Required Thick. (inch)	0.0500		
	Required Tolerance(+)	10%		
	Required Tolerance(-)	10%		
	Measured epoxy/icon	0	(conductor - 0, epoxy -1)	
	PCB	PCB+HS		
	Final	HS+	After Freq.	
אץ לגעת בשורה מסתרה	Max.	0.0550	0.0000	0.0490
		0.0450	0.0000	0.0420
	Nominal Before Plating	0.0455		HS
	Design	0.0432	0.0000	0.0000
			PP	PCB+HS stackup
			0.0000	0.0000
				<a href="#">OLD MASTER Eltek-Material.XLS</a>
	DATE	28/1/2020		
	UP DATE			
	Producer	Rogers		
	Designer	Amir		
	Material type	RT5880		
	Panel size	1208 MLG		
	No. of Nos. in pan.			
	No. of PCB in Nos.			
	No. of PCB panel.	3		

	Layer No.	Layer Descr.	.Cu (OZ)	CORE Thickness (inch)	Quantity	.Prep Thick. (inch)	.Dielec .Req. (micron)	drill kind	Control & Note's
	1	CS	0.5						
1/PD1	CORE		0.01				TF5742		
	PD1	0	0						
	2	G	0.5						
2/3	CORE		0.01				TF5742		
	3	S	0.5						
	PD4	0	0						
PD4/4	CORE		0.01				TF5742		
	4	G	0.5						
	PD5	0	0						
PD5/5	CORE		0.01				TF5742		
	5	PS	0.5						

RT5880 @ 10GHz Dk 2.20±0.02; Df 0.0009

Press temperature 370°C

Pressure 500 PSI

# Eltek BondPly StackUp RT5880



## CROSS SECTION REPORT

Customer Name: \_\_\_\_\_ Part No.: EL-F5703 Rev: \_\_\_\_\_  
 Eltek No.: 340011 Date Code: \_\_\_\_\_ Sample No.: \_\_\_\_\_  
 Total Thickness – Designed: 0.0432" Measured: \_\_\_\_\_

### Construction

	Layer	Layer	.Cu (OZ)	CORE Thickness (inch)	Quantity	Prep	Dielec		drill kind
	No	Disp				Thick	Req		
						(inch)	(microns)		
	1	CS	0.5						
1/PD1	CORE		0.01					TF5742	
	PD1	0	0						
	2	G	0.5						
2/3	CORE		0.01					TF5742	
	3	S	0.5						
	PD4	0	0						
PD4/4	CORE		0.01					TF5742	
	4	G	0.5						
	PD5	0	0						
PD5/5	CORE		0.01					TF5742	
	5	PS	0.5						

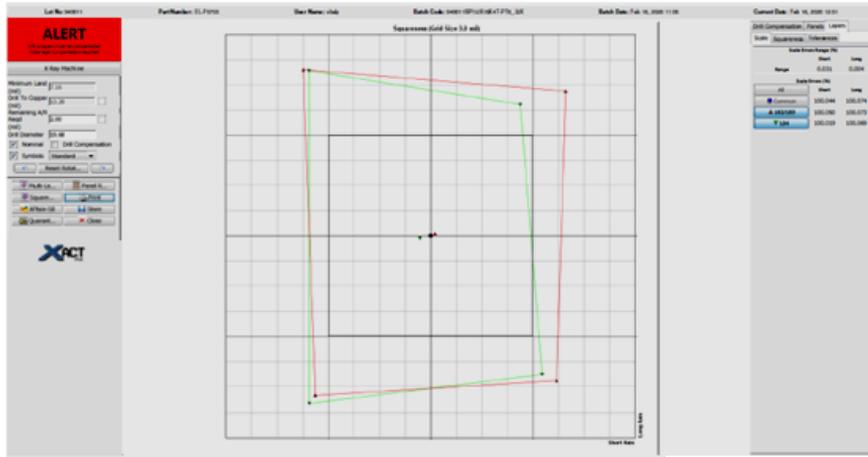
	Designed (µm)		Measured (µm)	
	Copper Layer	Dielectric	Copper Layer	Dielectric
1		254		240
2		254		244
3		254		234
4		254		242
5				
6				
7				
8				

G  
S  
S

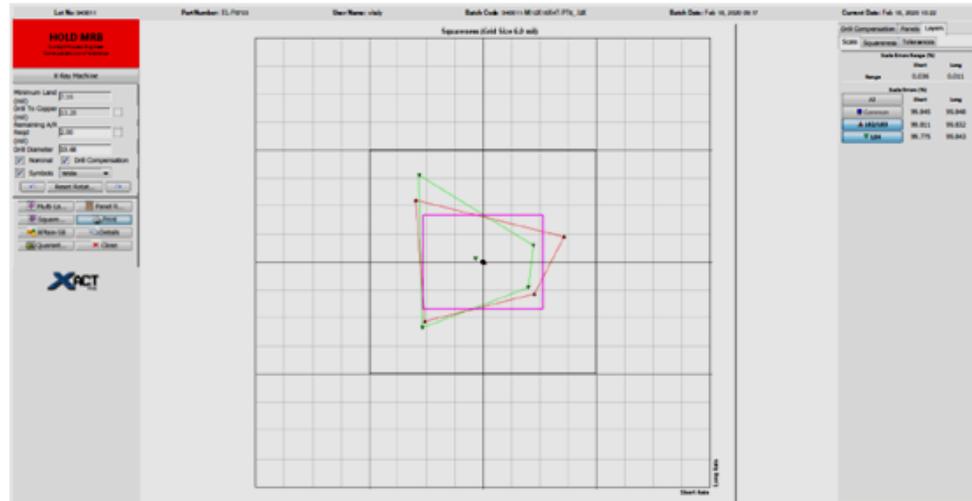
# Registration RT5880

Before Lamination

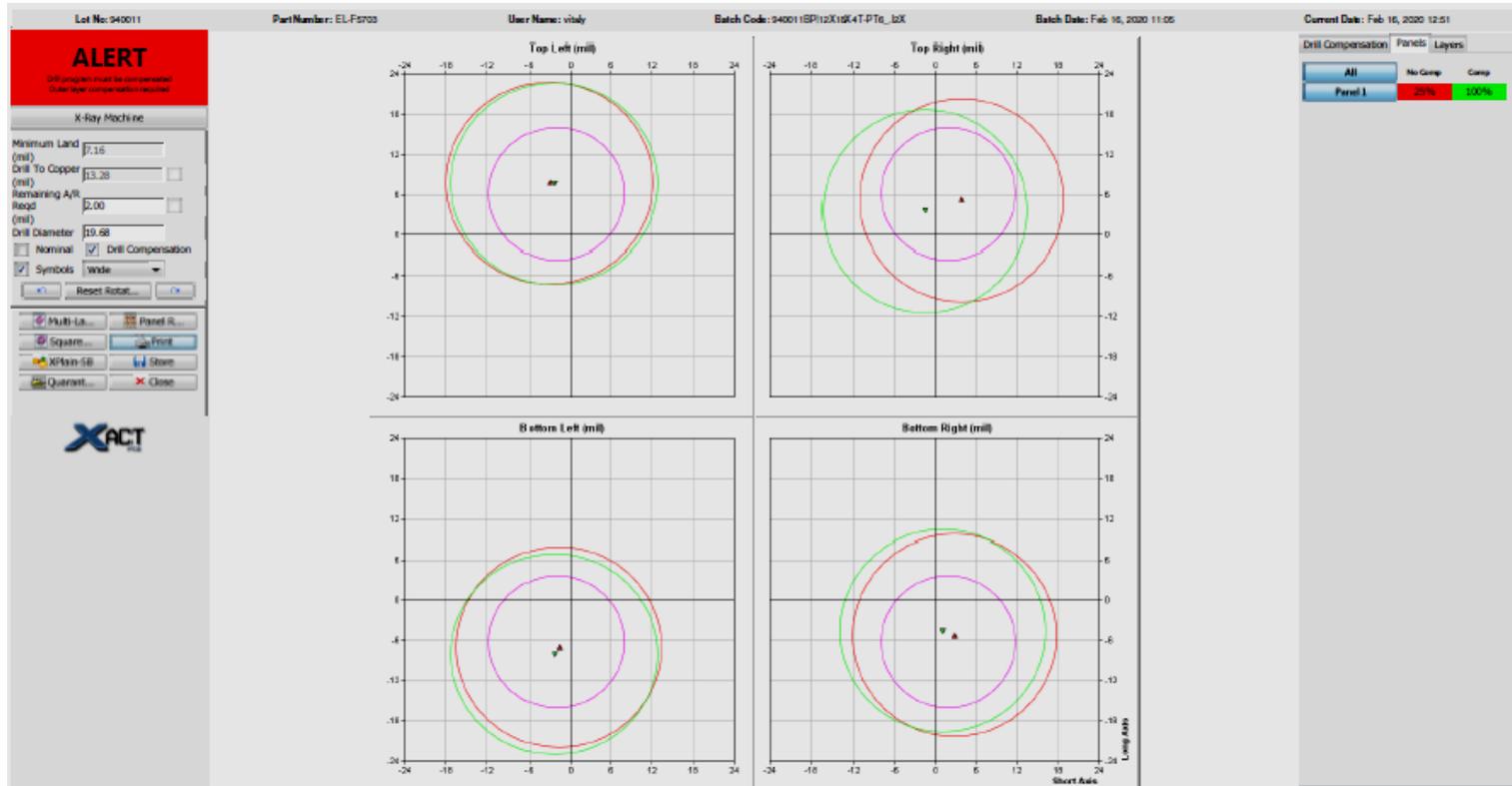
(Layup done on 4 slots Multi-Line system and riveting with 8 rivets)



After Press

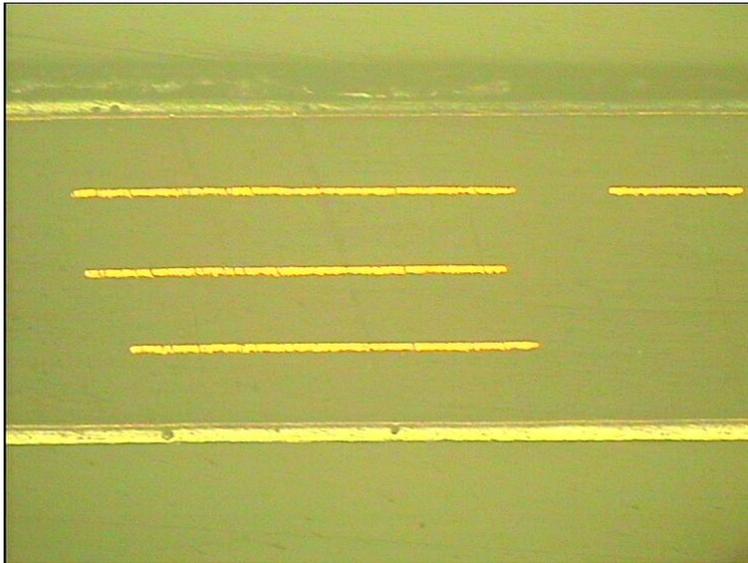


# Registration RT5880

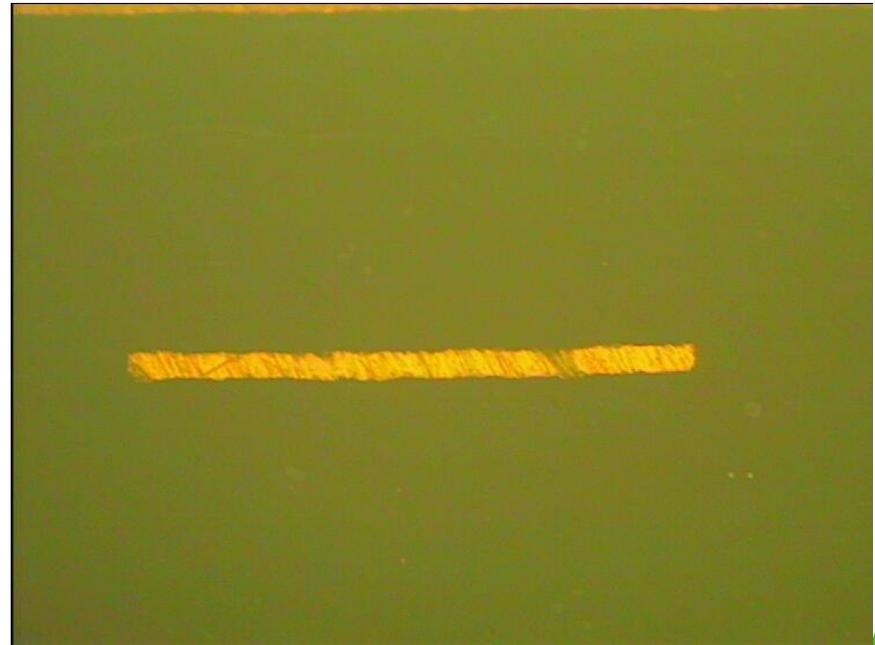


- ✓ Good centering position
- ✓ Good layer to layer registration

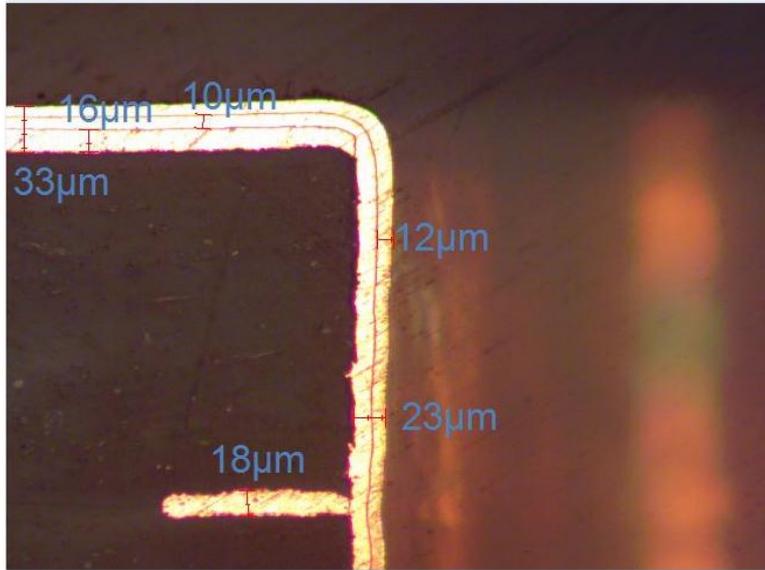
# Coupon Tests RT5880



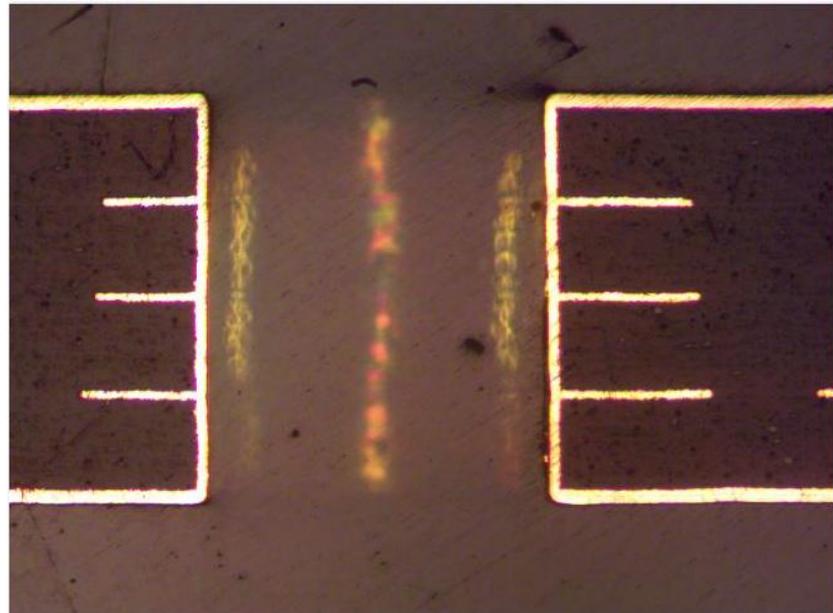
After Press



# Coupon Tests RT5880

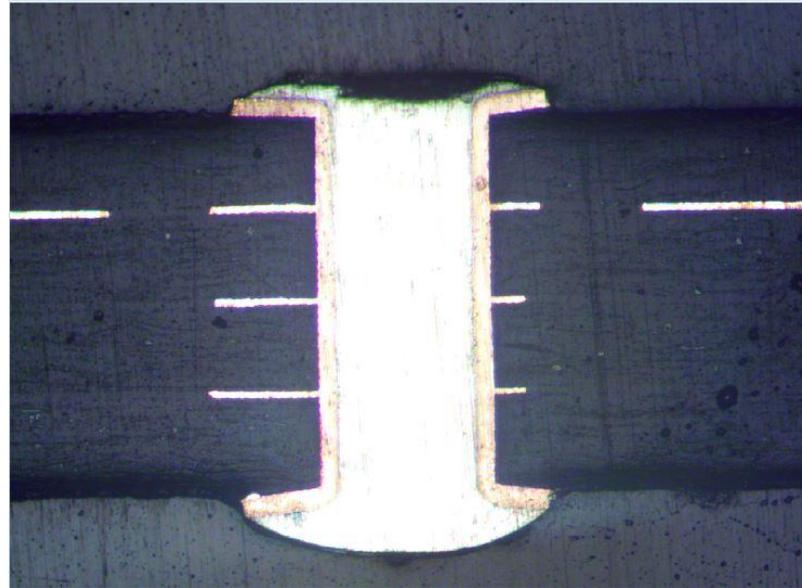
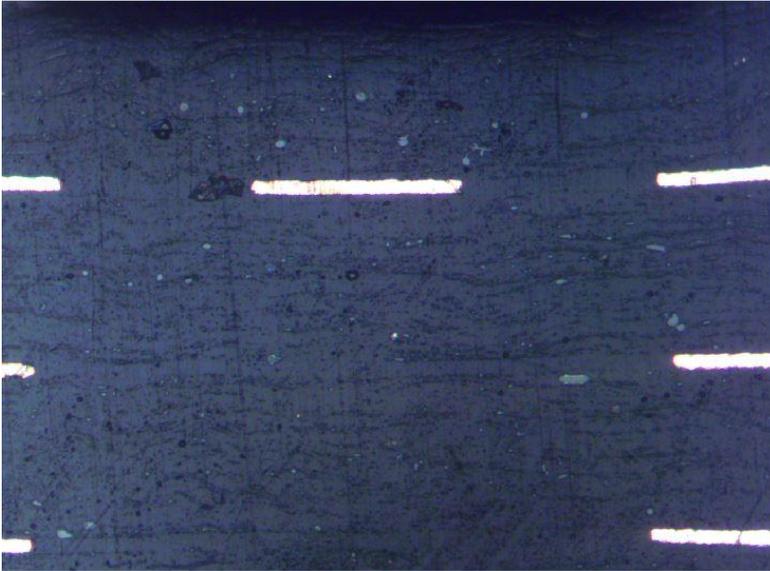


After Cu Plating

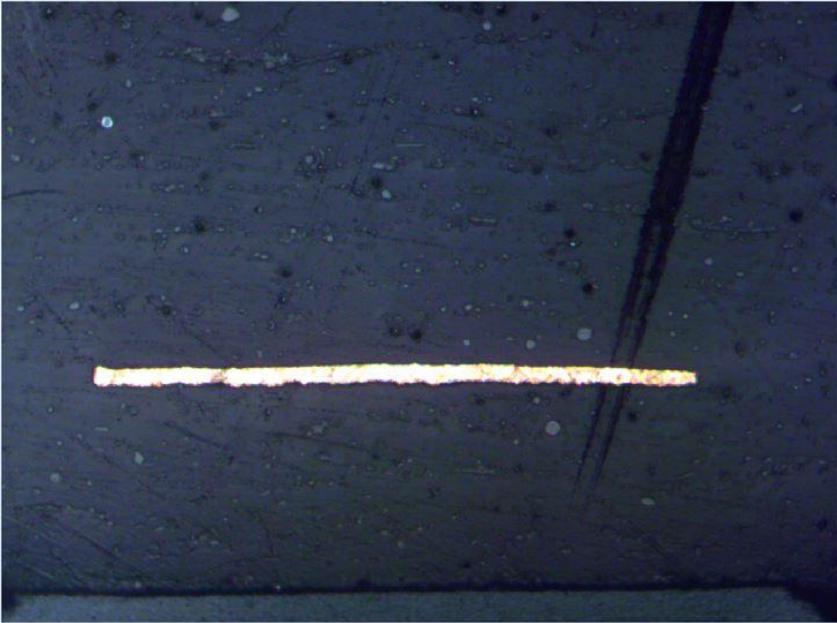


# Coupon Tests RT5880

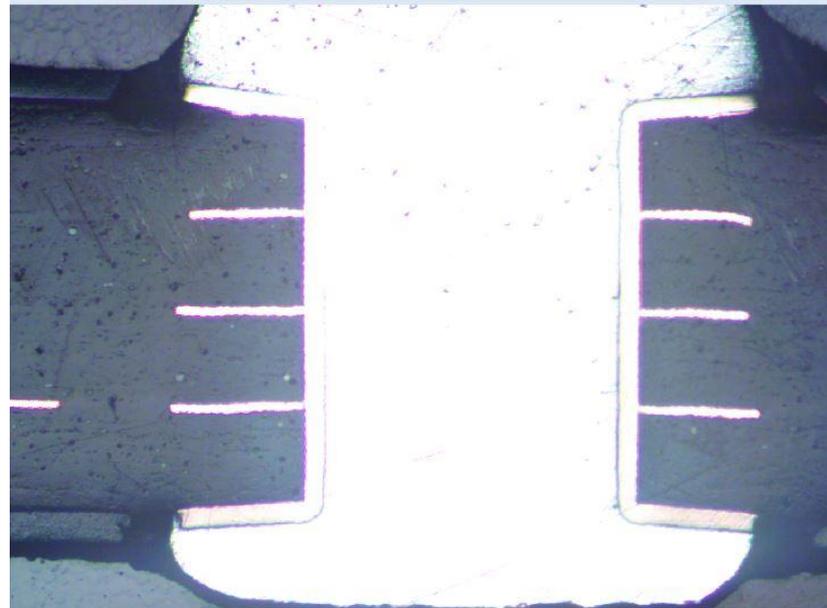
After 3 Thermal Stresses  
@285°C x 10 sec x 3 times



# Coupon Tests RT5880



After 6 Thermal Stresses  
@285°C x 10 sec x 6 times



# Eltek Capability PTFE Fusion Bonding

- ✓ Panel Size 12"x18"
- ✓ Bond Ply and Direct Bonding Process
- ✓ Core Material: [Rogers RT6002, RT5880](#)
- ✓ Bond Ply Materials: [Rogers RO3003](#)
- ✓ High Thermal Stress Reliability



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# Eltek Roadmap for PTFE Fusion Bonding

- Panel Size 12"x18"
- Direct Core to Core Lamination (**Rogers Materials**)

Material	Dk@10GHz	Df@10GHz
RO1200 ceramic-filled laminates reinforced with woven fiberglass	3.05	0.0017
CLTE MW ceramic filed, woven glass reinforced PTFE	2.94÷3.02±0.04 Depend on the thickness	0.0015

- Bond Ply Construction (**Rogers Materials**)

CCL	BondPly
RO1200	RO1200BP

- Liquid to Liquid Test for PTFE Fusion Bonded MLPCB

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# Eltek Roadmap for PTFE Fusion Bonding

- Panel Size 12"x18"
- Direct Core to Core Lamination (**Taconic Materials**) :

Material	Dk@10GHz	Df@10GHz
NF-30 PTFE non-reinforced ceramic-filled	3.0±0.04	0.0013
TLY-5 PTFE reinforced with very lightweight woven fiberglass	2.20±0.02	0.0009
TSM-DS3 ceramic-filled reinforced material with very low fiberglass content (~ 5%)	3.00	0.0011

- Direct Core to Core Lamination (**Ventec Material**):

Material	Dk@10GHz	Df@10GHz
Tec-Speed 30.0 L300 [VT-3703] Ceramic filled PTFE composites	3.0±0.04	0.0009

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Thank you



# Sources of Information

1. [www.microwavejournal.com/blogs/1-roq-blog/post/20670-fusion-bonding-forms-reliable-multilayer-circuits](http://www.microwavejournal.com/blogs/1-roq-blog/post/20670-fusion-bonding-forms-reliable-multilayer-circuits).
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