

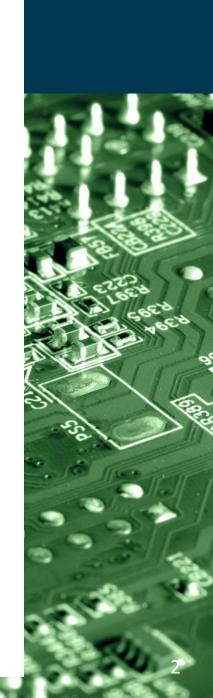




Company Profile

- Leading manufacturer of complex flex rigid and high-density rigid PCBs for advanced high reliability applications.
- Markets Served:
 - Defense
 - Space
 - Aerospace
 - High Rel Medical
 - Oil & Gas / Industrial
 - Research
- Established in 1970
- Publicly traded on Nasdaq (ELTK)





Company Profile

Factory Information

Location



Petah Tikva, Israel

Size



100,000 ft²

Employees



295

- (12) Process Engineers
- (22) Product Engineers
- (12) Sales & Tech Support
- (20) QA
- (27) Leadership / Management
- (~205) Production

2 Shifts; 5 days a week

Revenues 2019



34.8 M

Main Products



Flex Rigid



Rigid



Multi-Flex / Flex

<800,000 PCBs

Key Qualifications



NADCAP, AS9100D, ISO9001:2015. UL 94V-0

Manufacturing Capabilities





Main Product Types

Flex Rigid, Rigid, Multiflex and Flex



Panel Sizes

12x18, 18x24, Backplane Panel (Max Board Size – 19" x 26")



Max Layers

38 layers +; max thickness 0.252" (6.4mm)



Copper Weights

- Base copper down to 5 microns
- Max Copper Thickness: 4 oz



Materials

DuPont, Rogers, Iteq, Ventec, Panasonic, Arlon, Isola and others

- Long experience with processing and mixed material type constructions
- Duroid Experience: 6002, 6006, 6010, 6202, 5870, 5880
- Fusion Bonding of pure Teflon (PTFE)
- Teflon on Brass
- Flexible Silver Shielding

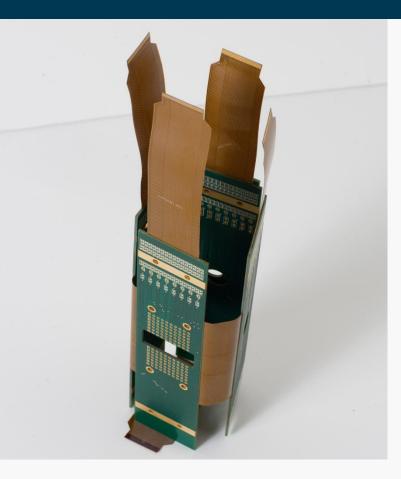


HDI

- Stacked / Staggered Microvias
- Sequential Build up to: 5+N+5
- Via Filling: Via In Pad, Microvia Fill, Copper Fill



Manufacturing Capabilities





Laser Direct Imaging & Direct Image Solder Mask

Film free factory; all product is direct imaged



Soldermask

Green, Blue, White, Red & Black



AOI

All inner layers and outer layers 100% AOI Inspected



Controlled Depth NC Processing

- Back Drilling, Cavity Formations, Edge Castellation, Controlled Depth Milling
- Embedded COIN technology



Heatsinks & CTE Solutions:

- 3D wrap around, Internal, External
- Built in Ceramic Substrate



Electrical Testing:

• 100% by flying probe



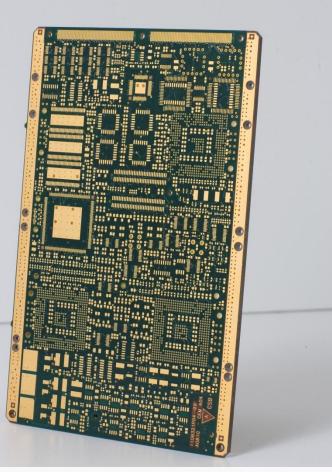
Surface Finishes:

- HASL, ENIG, Immersion Ag, Hard Au
 / Soft Au all processes in house
- Currently subcontract ENEPIG* volume warrants in-house installation

*For export restricted product MLA amendment has been approved by DDTC and BIS to give us the ability to use our subcontractor for ENEPIG and other specialty finishes.



Manufacturing Capabilities





Exact drilling capabilities

- DOP- drill on pad. Precise drilling using CCD camera
- X-Ray assisted registration & drilling for complex PCBs.
- Individual drilling file for PCB in production panel.

Special mechanical drilling capabilities

3&4 mil diameter TH

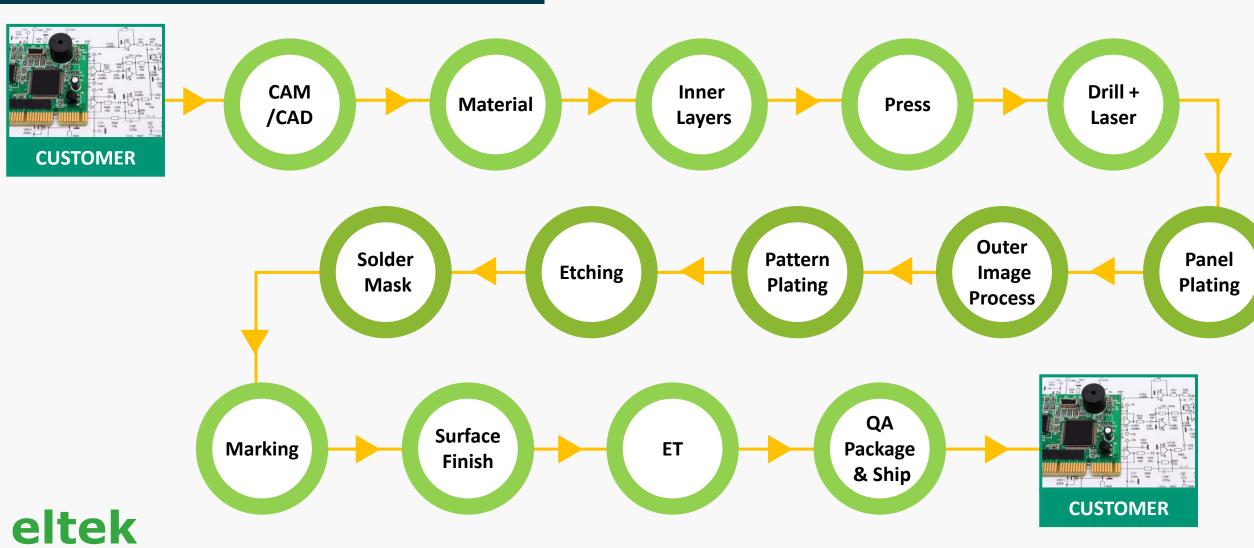


- 100% by flying probe
- 16 Test Heads "ATG A7-16 XW Flying Probe Test System"
- High Speed Direct Linear Drives for X and Z motion
- Light weight Carbon Z-Axis
- Test System for oversized panels up to 1000 mm
- Fast 300 mA Kelvin Testing
- Capacitor test up to 1000V



Process Flow

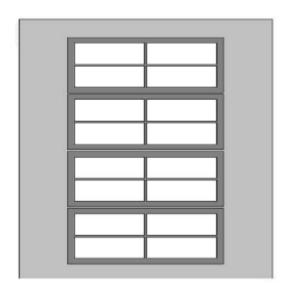
a Nistec company



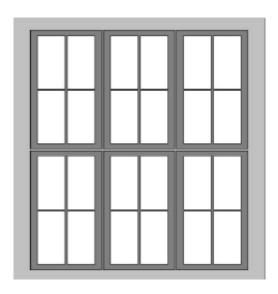
BASIC COSTS OF PRINTED CIRCUITS BOARDS



Production Panel Utilization Is An Important Cost Factor



Poor utilization 58%

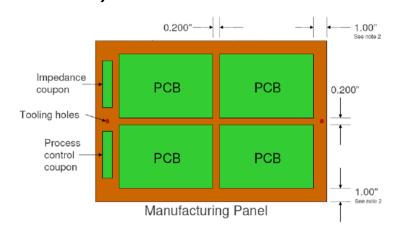


Good utilization 77.8%



Quality approvals and controlled impedance require extra coupons

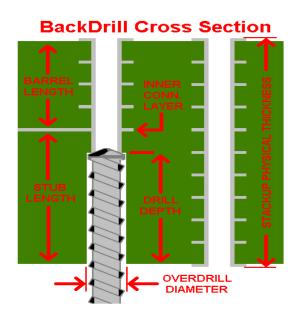
- ✓ IPC Class 3 (Multiple industries)
- ✓ AS9100D (Aerospace & Avionics)
- ✓ Mil-P-55110 (Military)
- ✓ ISO 13485 (Medical)





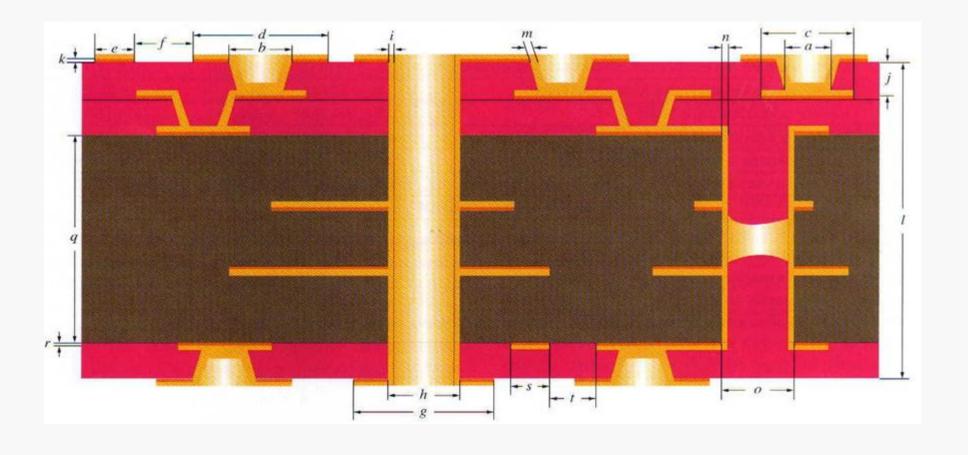
Drilling Process

- ✓ Number of drilled holes
- ✓ Min. drilled diameter
- ✓ Number of diameters





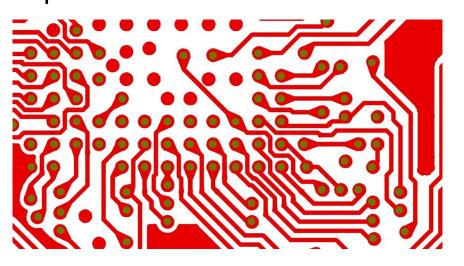
HDI via between layer 1-2 and 2-3 with buried vias





> Yield

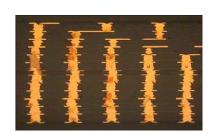
- ✓ Design features/complexity determine the yield thus costs.
- ✓ The predicted yield determines the number of production panels.

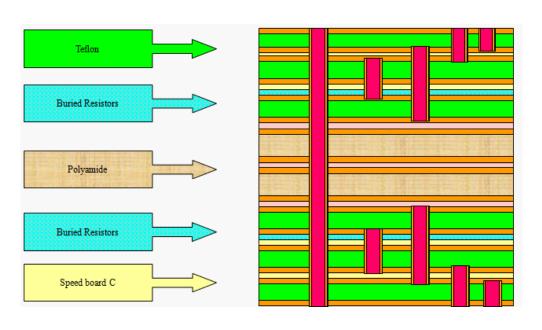




Cost Increase Factors

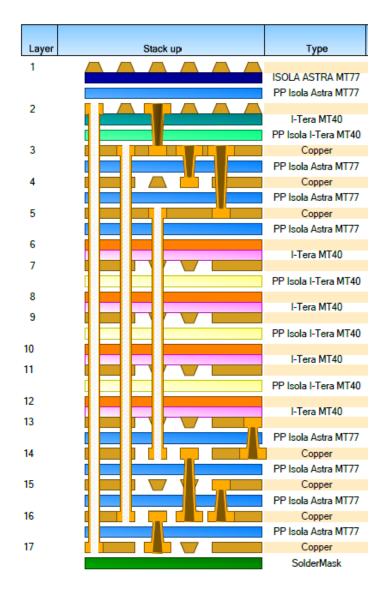
- Non- standard design rules
- ✓ Blind Via's, buried Via's, stacked Via's
- ✓ Resin filling and capping Via's
- ✓ Back drill







Cost Of Press Factors





Summary

- ✓ Production panel utilization
- ✓ Drilling process
- Design rules
- ✓ Blind & Buried Via's
- Costs Press Factors







